



AF/IFW #

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Atty Dkt. 550-499
C# M#

TC/A.U.: 2863

Examiner: Walling, Meagan S.

Date: March 31, 2006

re Patent Application of

HOULIHANE

Serial No. 10/743,473

Filed: December 23, 2003

Title: GENERATION OF A TESTBENCH FOR A REPRESENTATION OF A DEVICE

Mail Stop Appeal Brief - Patents

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL**

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences

from the last decision of the Examiner twice/finally rejecting applicant's claim(s). \$500.00 (1401)/\$250.00 (2401) \$

☒ An appeal **BRIEF** is attached in the pending appeal of the above-identified application \$500.00 (1402)/\$250.00 (2402) \$ 500.00

☐ Credit for fees paid in prior appeal without decision on merits -\$ ()

☐ A reply brief is attached. (no fee)

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s)
One Month Extension \$120.00 (1251)/\$60.00 (2251)
Two Month Extensions \$450.00 (1252)/\$225.00 (2252)
Three Month Extensions \$1020.00 (1253)/\$510.00 (2253)
Four Month Extensions \$1590.00 (1254)/\$795.00 (2254) \$

☐ "Small entity" statement attached.

Less month extension previously paid on -\$ ()

TOTAL FEE ENCLOSED \$ 500.00

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140**. A duplicate copy of this sheet is attached.

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Signature: 



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A DEVICE

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BRIEF FOR APPELLANT

**On Appeal From Final Rejection
From Group Art Unit 2863**

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APPEAL BRIEF

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, ARM Limited, a United Kingdom corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals related to this subject application. There are no interferences related to this subject application.

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III. STATUS OF CLAIMS

Claims 1-46 are pending. Claims 5, 6, 8-17, 19-21, 29, 30, 32-41, and 43-45 have been indicated as allowable. Claims 1-4, 7, 18, 22-28, 31, 42, and 46 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication U.S. 2004/0111252 to Burgun et al. Claims 1-4, 7, 18, 22-28, 31, 42, and 46 are appealed.

IV. STATUS OF AMENDMENTS

No amendment has been filed after final.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

When developing components or devices for integration into a system, a number of test procedures are typically performed to ensure that the device will operate in the desired manner when integrated into the system. The development of a device includes defining a representation of its functional operation and then synthesizing the device representation into a sequence of hardware elements using a synthesizing tool. The result of the synthesis is a device design that can be used to produce the actual hardware device. A testbench model may be used to test the device representation. The testbench model provides a test environment for the device representation and is run on a simulation tool to produce test results which

can be analyzed to determine whether the device representation is operating as required.

If a particular instantiation of a configurable device representation is produced based on some specific configuration data, the representation may be placed within a larger system representation that includes representations of other interacting devices. But in this situation, direct control over the input stimuli to the representation of the specific device being tested is lost, resulting in a less than satisfactory test procedure. See page 3, lines 4-10.

As a non-limiting example, the System on Chip (SoC) design 10 in Figure 1 shows devices 15, 20, 25, 35 and 45 interconnected by buses as specified within an interconnect block 60—the device whose design and testing is highlighted in the following example. See page 11, beginning at line 19. The interconnect block 60 includes a bus matrix which provides for the interconnection of multiple bus masters and slaves within the SoC 10. Each master device can access a different subset of the slave devices, and may also use a different memory map. Further, each slave can use one of a number of different arbitration schemes. For any particular instantiation of the interconnect block 60, various parameters will be defined. But in general, there are thousands of possible configurations of the interconnect block. See page 13, line 30-page 14, line 7.

The whole of the SoC design 10 will typically be defined in a Register Transfer Language (RTL) representation, and each device in Figure 1 can be

considered as a separate RTL device representation. Each device RTL representation must be tested, either alone or in combination with other device RTL representations, by constructing a testbench around the device representations to provide a test environment for subsequent execution on a simulator tool. This verification process accounts for a significant proportion of the total design effort. See page 13, lines 3-4.

The interconnect block design 60 is intended to be configurable, so that the same basic design can be used in a number of different implementations. But the flexibility in the design of the interconnect block adds to the complexity of verifying the generated design. Given the potentially complex interactions in the design, generating a suitable test sequence to fully exercise a generic interconnect block design is a difficult task, and will not typically verify that all possible instantiations of the interconnect block 60 will always produce a correctly functioning interconnect block. See page 13, lines 9-18.

Although a particular instantiation of the interconnect block 60 can be tested in the context of the SoC design, (see Figure 2), that approach only allows indirect control of the input stimuli to the interconnect block, and therefore, all possibilities of transactions via the various interconnection of buses cannot be tested. See page 3, lines 19-29. The interconnect block 60 could be tested in isolation, as illustrated in Figure 3, with a matching testbench 100 being generated for any particular instantiation of the interconnect block 60. But this approach is

normally prohibitive because a specific testbench 100 must be written for each of possibly thousands of instantiations of the interconnect block 60. See page 13, lines 30-page 14, line 4. The inventor conceived of a technique to automatically produce a matching testbench 100 for any particular instantiation of the interconnect block 60. See page 14, lines 4-7.

Figure 4 (reproduced below) shows a processing tool 150 for generating both a representation of a device under test (DUT) 170 (in the above example an interconnect block) and a matching testbench representation 175. A first set of templates 160 is used in generating the testbench 175, and a second set of templates 165 is used in generating the DUT 170. See page 14, lines 8-11.

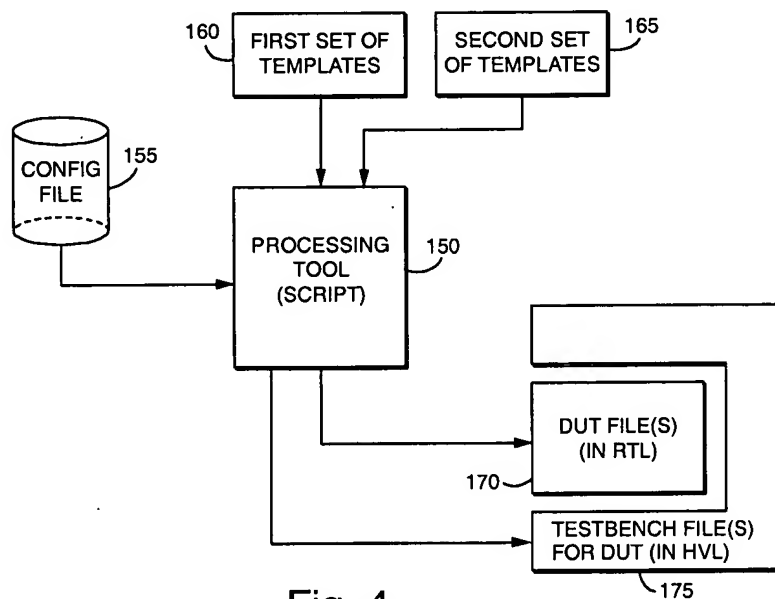


Fig. 4

The second set of templates 165 used by the processing tool to generate the DUT representation 170 includes definitions for each constituent block of that DUT.

The non-limiting example in Figure 5 includes definitions of an input stage, an output stage, a decoder, a multiplexer, etc. For any particular instantiation of the device, the designer specifies a configuration file 155 providing the information required to enable the processing tool to build a representation of that required device from the second set of templates 165. See page 15, lines 1-5.

In one non-limiting example embodiment, the processing tool 150 is a script which processes the constructs provided within the second set of templates with reference to the configuration file 155 to produce one or more files defining the device representation e.g., in RTL. See page 15, lines 9-13. The script 150 also reads a first set of templates 160 and applies the same configuration file 155 to produce one or more output testbench files defining a testbench representation matched to the particular instantiation of the device representation produced using that configuration file 155. An example of the testbench produced for the interconnect block illustrated in Figure 5 is shown in Figure 6 permitting direct control of the testing inputs.

Figure 8 illustrates an example overall process for generating a device representation and a matching testbench representation and then running a simulator to produce test results. See page 19. The processing tool 150 reads the configuration file 155 and generates one or more DUT files with reference to the second set of templates 165. One or more testbench files are generated by the processing tool 150 with reference to the first set of templates 160. When a

simulator tool is later run, it reads out the DUT and testbench representation files and performs a simulation to generate some output results.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

All rejections are requested for review on appeal. Specifically, the rejection of claims 1-4, 7, 18, 22-28, 31, 42, and 46 under 35 U.S.C. §102(e) as being anticipated by Burgun is appealed.

VII. ARGUMENT

A. Legal Standard for Anticipation

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Burgun fails to satisfy this exacting standard.

B. Burgun Describes An Emulation/Simulation Platform

In paragraph 0002, Burgun states that his invention applies to "the implementation of a test environment for a circuit whose operation one seeks to validate (and referred to as the 'design under test') and which is *emulated* entirely

or partly by a reconfigurable hardware system." Burgun explains that "emulator" means "a reconfigurable hardware system." Paragraph 0003.

Because the test environment embedded in the reconfigurable hardware system and the design under test are both typically implemented by the same configurable resources, Burgun sees a problem with the "very strong dependence between the test environment and the design under test." Paragraph 0017. Burgun's solution is a simulation/emulation platform in which the reconfigurable system emulating the design under test is separated from that emulating the hardware part of the test environment. See paragraphs 0023-25.

C. Burgun Does Not Disclose Generating A Device Representation and A Testbench Representation

Claims 1 and 25, for example, recite:

- "generating a testbench *for a representation* of a device to be incorporated in a data processing apparatus,"
- "the *testbench* providing a test environment that *represents* one or more components of the data processing apparatus with which that device is to be coupled,"
- "the *representation* of the device being configurable based on configuration data specifying predetermined attributes of the one or more components."

Claims 23 and 46 similarly recite:

generating a representation of a device ... and a
testbench ... that represents one or more components

of the data processing apparatus with which that device is to be coupled, the representation of the device being configurable in dependence on the one or more components.

Burgun lacks these features recited in the independent claims because Burgun is focused on a different phase in device design testing. Burgun starts off with an *already-generated* design under test and an *already-generated* associated test environment. For example, Burgun states in paragraph 0026: "the invention therefore proposes a method of emulating a design under test associated with a test environment." Paragraph 0076 states that the system in Figure 1 of Burgun "includes an emulator of the design under test EML and an assembly ENVT embodied as a test environment for this same design under test." A design under test, i.e., the representation of a device under test, has already been generated. There is even an emulator for that design. Similarly, the reconfigurable test bench BTR is part of an already existing "assembly ENVT."

It is in this context that paragraphs 0027-29 must be understood. Assuming an already-generated design under test and an already-generated test environment, Burgun configures reconfigurable hardware circuits to simulate/emulate the operation of that design under test and associated test environment. Thus, Burgun relates to the simulation process described on page 6, lines 12-16.

In contrast, claims 1, 23-25, and 46 are directed to the *earlier* phase of generating a representation of the device under test and a representation of its

associated test environment, so that those representations can subsequently be simulated using a simulation tool. The Board should consider the non-limiting example sequence of steps shown Figure 8 of the instant application (reproduced below) where steps 605-615 are performed by a processing tool 150 to generate files for a representation of a device under test (DUT) (see step 610) and files for a representation of a test bench file (see step 615) using the *same* configuration data for the DUT representation.

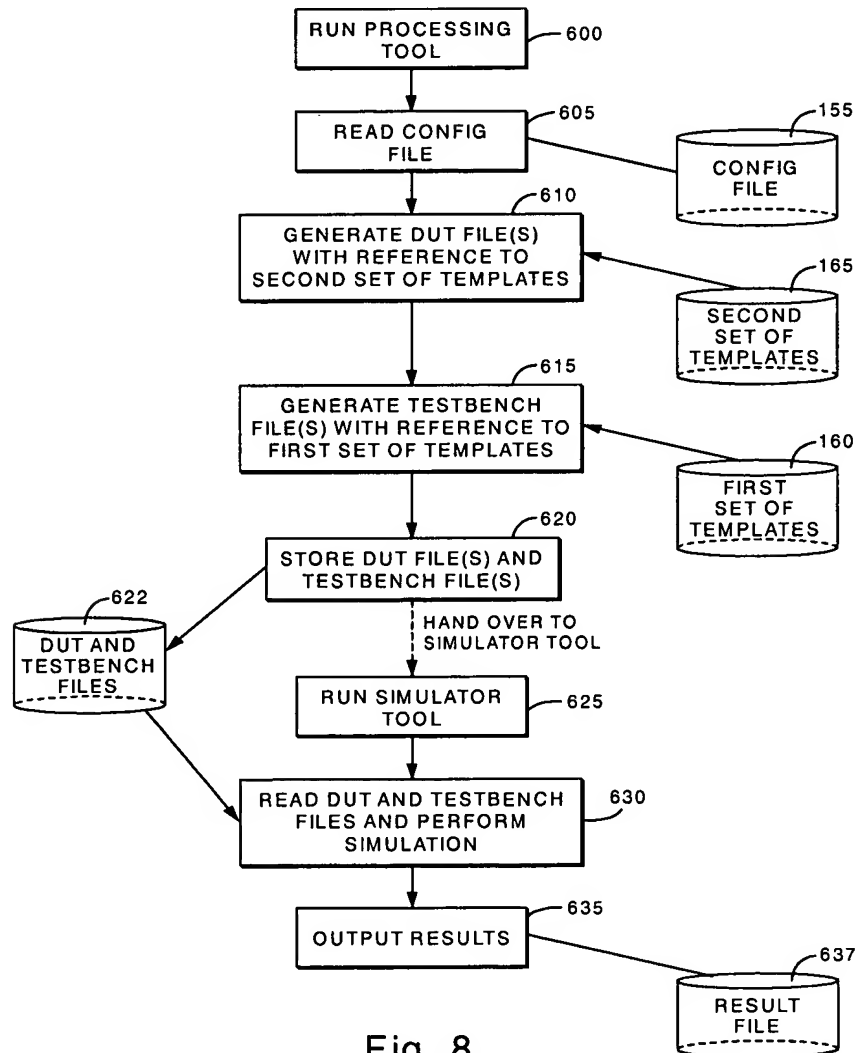


Fig. 8

Only after these two sets of representation files have been generated is a simulator tool run (step 625) and simulation performed using those generated file sets (step 630). Each of the *independent* claims is directed to generating these files. Simulation using those files is explicitly recited in *dependent* claims. See for example dependent claim 8. So it is unreasonable to argue that the independent claims can be construed as simulation since a dependent claim adds simulation.

D. Burgun Does Not Disclose Receiving the Configuration Data Used to Configure the Representation of the Device and Generating the Testbench with Reference to the Configuration Data

Claims 1 and 23 recite "receiving the configuration data used to configure the representation of the device" and "generating the testbench with reference to the configuration data and a first set of templates defining the test environment." These features are not described in Burgun.

As demonstrated above, Burgun assumes the existence of the design under test and the test bench BTR. Although both were generated in some fashion, Burgun does not describe how they were generated. There is no disclosure that the test bench BTR was generated based on configuration data used to configure the design under test or a set of templates defining a test environment. The test bench exists. The Examiner fails to point out where Burgun describes ever

receiving any kind of data—let alone the claimed configuration data and the first set of templates—used to generate the test bench BTR.

Accordingly, Burgun's configuration files are not used to "configure the representation of the device" (quoted from claim 1) and to generate the associated "testbench with reference to the configuration data and a first set of templates defining the test environment" (quoted from claim 1). Instead, Burgun's configuration files are used to configure the reconfigurable hardware units for emulating an *already-existing* design under test and an associated test environment.

E. Burgun Does Not Disclose Generating the Testbench with Reference to the SAME Configuration Data Used to Configure the Representation of the Device

The independent claims require that the test bench be generated with reference to the same configuration data used to configure the representation of the device. For example, claim 1 recites at step (b) the testbench is generated with reference to the configuration data and a first set of templates. From the earlier recitations in claim 1, **the** configuration data being referred to is the same configuration data used to configure the representation of the device.

This feature of using the same configuration data as claimed is yet another claim feature missing in Burgun. The Examiner relies on paragraphs 0028 and 0032 of Burgun. Paragraphs 0026-30 describe emulating an already-generated

design under test with an already-generated test environment (see paragraph 0026). This emulation process involves generating two *different* configuration files. The first configuration file is used to configure a first reconfigurable hardware part that represents the already existing test bench BTR (paragraph 0028). The second configuration file is used to configure a second reconfigurable hardware part EML for emulating the design under test (paragraph 0029). As stressed in paragraph 0029, the first and second reconfigurable hardware parts are “distinct and mutually connected.” These two separate parts are provided with their own *separate configuration files* to overcome the problems associated with the “strong dependence” between the test environment and the design under test.” See paragraph 0017.

Indeed, Burgun *stresses the importance of using two different configuration files* (albeit used for different purposes than generating representations of a device and testbench). The first configuration file configures the reconfigurable hardware representing the testbench and the second configuration file configures the reconfigurable hardware unit acting as an emulator for the device under test. See, for example, Burgun's criticism of a strong dependence between the test environment and the design under test in paragraph 0017 and Burgun's contrasting approach where the two are “separated.” Paragraph 0025.

Unlike Burgun, the inventor in this application recognized the value in having the same configuration data be used in generating the representation of the device under test and the representation of the testbench. As a result, it is possible to automatically generate testbench representation files for the device under test (DUT) that match the top-level of the representation of the DUT. This allows any possible configuration of the DUT to be tested when that particular configuration of the DUT has been generated.

F. Burgun Does Not Disclose Generating the Testbench Representation with Reference to Both the Same Configuration Data Used to Configure the Device Representation and a First Set of Templates

The independent claims recite generating "the testbench with reference to the configuration data and a first set of templates defining the test environment." As explained already, Burgun's testbench is assumed to already exist. It has been generated, but Burgun does not explain how. Nor does the Examiner explain where or how Burgun generates the testbench BTR using a "first set of templates defining the test environment."

The Examiner refers to paragraph 0032 in relation to step (b) of claim 1, but does not explain what element in Burgun corresponds to the first set of templates. It is unclear whether the Examiner is taking the position that compilation directives are analogous to the claimed first set of templates. If that is the case, such a position is inconsistent with Burgun's teachings in paragraph 0032

where using the compilation directives results in the first configuration file (see the last line of paragraph 0032). But in claim 1, the first set of templates and the configuration data are used as inputs in generating a new testbench representation rather than configuring an already-existing testbench representation. Paragraph 0032 in Burgun also makes clear that the configuration file is the output of the processing and not an input. Accordingly, the compilation directives being referred to in paragraph 0032 are entirely different than the first set of templates recited in the independent claims.

G. Burgun Does Not Disclose Generating the Device Representation with Reference to Both the Same Configuration Data Used to Configure the Device Representation and a Second Set of Templates

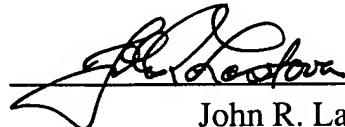
Claims 23 and 46 also recite using "the processing tool to generate the representation of the device with reference to the configuration data and a second set of templates defining the representation of the device." This feature is not disclosed in Burgun. The Examiner fails to explain where or how Burgun generates a representation of the device under test using "second set of templates defining the representation of the device." Burgun's device representation has already been generated, but Burgun does not say how. Nor does the Examiner specifically identify what element in Burgun supposedly corresponds to the claimed second set of templates.

VIII. CONCLUSION

The Examiner's final rejection never specifically addresses the multiple distinctions between the independent claims and Burgun previously pointed out by Appellant. Instead, the Examiner argues that while the technology described in the instant specification is novel, that novelty is not recited in the appealed claims. But as clearly demonstrated above, there are multiple phrases recited in the independent claims that simply are not disclosed in Burgun. Simply stating that the claims are "broader" that what is described in the specification is not enough to demonstrate anticipation. Rather, the Examiner must identify where and explain how each claim feature is described in Burgun. The Examiner fails to meet that burden. Given the fact that multiple features recited in the independent claims 1, 23, 25, and 46 are missing from Burgun, the Board should reverse the outstanding anticipation rejection.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
John R. Lastova
Reg. No. 33,149

JRL/sd
Appendix A - Claims on Appeal



IX. CLAIMS APPENDIX

A method of generating a testbench for a representation of a device to be incorporated in a data processing apparatus, the testbench providing a test environment that represents one or more components of the data processing apparatus with which that device is to be coupled, the representation of the device being configurable based on configuration data specifying predetermined attributes of the one or more components, the method comprising the steps of:

- (a) receiving the configuration data used to configure the representation of the device; and
- (b) generating the testbench with reference to the configuration data and a first set of templates defining the test environment.

2. A method as claimed in Claim 1, further comprising the step of:

- (c) generating the representation of the device with reference to the configuration data and a second set of templates defining the representation of the device.

3. A method as claimed in Claim 2, further comprising the step of:

providing a processing tool having access to the configuration data and the first and second sets of templates, said steps (b) and (c) being performed by the processing tool.

4. A method as claimed in Claim 3, wherein the processing tool is operable independent of a language produced by the processing tool from each template.
7. A method as claimed in Claim 1, wherein said device is a bus interconnect block.
18. A method as claimed in Claim 2, wherein the representation of the device is formed from constituent blocks and the second set of templates defines the representation of the device and its constituent blocks.
22. A computer program product comprising code portions operable to control a computer to perform a method as claimed in Claim 1.
23. A method of generating a representation of a device to be incorporated in a data processing apparatus and a testbench providing a test environment that represents one or more components of the data processing apparatus with which that device is to be coupled, the representation of the device being configurable in dependence on the one or more components, the method comprising the steps of:
- (a) receiving a configuration data specifying predetermined attributes of the one or more components;
 - (b) employing a processing tool to generate the testbench with reference to the configuration data and a first set of templates defining the test environment; and

(c) employing the processing tool to generate the representation of the device with reference to the configuration data and a second set of templates defining the representation of the device.

24. A computer program product comprising code portions operable to control a computer to perform a method as claimed in Claim 23.

25. A system for generating a testbench for a representation of a device to be incorporated in a data processing apparatus, the testbench providing a test environment that represents one or more components of the data processing apparatus with which that device is to be coupled, the representation of the device being configurable based on configuration data specifying predetermined attributes of the one or more components, the system comprising:

logic operable to read the configuration data used to configure the representation of the device; and

generation logic operable to generate the testbench with reference to the configuration data and a first set of templates defining the test environment.

26. A system as claimed in Claim 25, wherein the generation logic is further operable to generate the representation of the device with reference to the configuration data and a second set of templates defining the representation of the device.

27. A system as claimed in Claim 26, further comprising:
a processing tool having access to the configuration data and the first and second sets of templates, the generation logic being provided by the processing tool.
28. A system as claimed in Claim 27, wherein the processing tool is operable independent of a language produced by the processing tool from each template.
31. A system as claimed in Claim 25, wherein said device is a bus interconnect block.
42. A system as claimed in Claim 26, wherein the representation of the device is formed from constituent blocks and the second set of templates defines the representation of the device and its constituent blocks.
46. A system for generating a representation of a device to be incorporated in a data processing apparatus and a testbench providing a test environment that represents one or more components of the data processing apparatus with which that device is to be coupled, the representation of the device being configurable in dependence on the one or more components, the system comprising:
logic operable to read a configuration data specifying predetermined attributes of the one or more components;

a processing tool operable to generate the testbench with reference to the configuration data and a first set of templates defining the test environment; and

the processing tool further being operable to generate the representation of the device with reference to the configuration data and a second set of templates defining the representation of the device.

X. EVIDENCE APPENDIX

There is no evidence appendix.

XI. RELATED PROCEEDINGS APPENDIX

There is no related proceedings appendix.